



# Arm<sup>®</sup> Neoverse<sup>™</sup> V3AE Core Cryptographic Extension

Revision r0p2

## Technical Reference Manual

**Non-Confidential**

**Issue 06**

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# Arm® Neoverse™ V3AE Core Cryptographic Extension Technical Reference Manual

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This document (102481\_0002\_06\_en) was issued on 2024-09-27. There might be a later issue at <https://developer.arm.com/documentation/102481>

The product revision is r0p2.

See also: [Proprietary Notice](#) | [Product and document information](#) | [Useful resources](#)

## Start Reading

If you prefer, you can skip to [the start of the content](#).

## Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the Neoverse™ V3AE core with the optional Cryptographic Extension.

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# Contents

**1. Cryptographic extension support in the Neoverse™ V3AE core.....4**

1.1 Product Revisions.....4

1.2 Disabling the Cryptographic Extension..... 4

1.3 Cryptographic Extensions register summary..... 5

1.4 ID\_AA64ISAR0\_EL1, AArch64 Instruction Set Attribute Register 0..... 5

1.5 ID\_AA64ZFR0\_EL1, SVE Feature ID register 0.....9

**Proprietary Notice..... 13**

**Product and document information..... 15**

Product status..... 15

Revision history..... 15

Conventions..... 17

**Useful resources.....20**

# 1. Cryptographic extension support in the Neoverse™ V3AE core

The Neoverse™ V3AE core supports the optional Armv8.0-A and Arm®v8.2-A Cryptographic Extension.

The Armv8.0-A Cryptographic Extension adds A64 instructions to Advanced SIMD that accelerate *Advanced Encryption Standard* (AES) encryption and decryption. It also adds instructions to implement the *Secure Hash Algorithm* (SHA) functions SHA-1, SHA-224, and SHA-256.

The Arm®v8.2-A extensions, Armv8.2-A-SHA and Armv8.2-SM, add A64 instructions to accelerate SHA2-512, SHA3, SM3, and SM4.

The SVE2-AES, SVE2-SHA3, and SVE2-SM extensions add A64 instructions to accelerate SHA3, SM3, SM4, and AES encryption and decryption.

## 1.1 Product Revisions

The following table indicates the main differences in functionality between product revisions.

**Table 1-1: Product revisions**

Revision	Notes
r0p0	First early access release
r0p1	First early access release for r0p1. Bug fixes only.
r0p2	First release for r0p2. Bug fixes only.

Changes in functionality that have an impact on the documentation also appear in [Revision history](#) on page 15.

## 1.2 Disabling the Cryptographic Extension

Disabling of the Cryptographic Extension applies to all Neoverse™ V3AE cores in a cluster.

To disable the Cryptographic Extension, assert CRYPTODISABLE.

When CRYPTODISABLE is asserted:

- Executing a cryptographic instruction results in an **UNDEFINED** exception.
- ID\_AA64ISAR0\_EL1 indicates that the Cryptographic Extension is not implemented.

### Related information

[1.4 ID\\_AA64ISAR0\\_EL1, AArch64 Instruction Set Attribute Register 0](#) on page 5

## 1.3 Cryptographic Extensions register summary

Software can identify the cryptographic instructions that are implemented in the Neoverse™ V3AE core by reading the identification registers.

The following table shows the instruction identification register for the Neoverse™ V3AE core Cryptographic Extension.

**Table 1-2: Cryptographic Extension register summary**

Name	Description
ID_AA64ISAR0_EL1	See 1.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0 on page 5
ID_AA64ZFR0_EL1	See 1.5 ID_AA64ZFR0_EL1, SVE Feature ID register 0 on page 9

## 1.4 ID\_AA64ISAR0\_EL1, AArch64 Instruction Set Attribute Register 0

Provides information about the instructions implemented in AArch64 state.

For general information about the interpretation of the ID registers, see *Principles of the ID scheme for fields in ID registers* in the [Arm® Architecture Reference Manual for A-profile architecture](#).

### Configurations

This register is available in all configurations.

### Attributes

#### Width

64

#### Functional group

Identification registers

#### Access type

See bit descriptions

#### Reset value

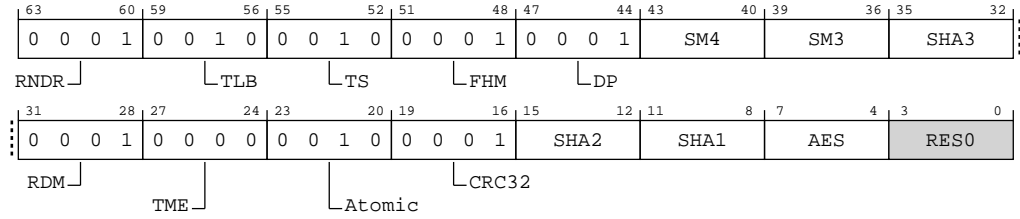
0001	0010	0010	0001	0001	xxxx	xxxx	xxxx	0001	0000	0010	0001	xxxx	xxxx	xxxx	xxxx
63	59	55	51	47	43	39	35	31	27	23	19	15	11	7	3
															0



Where the reset reads xxxx, see individual bits.

## Bit descriptions

**Figure 1-1: AArch64\_id\_aa64isar0\_el1 bit assignments**



**Table 1-3: ID\_AA64ISAR0\_EL1 bit descriptions**

Bits	Name	Description	Reset
[63:60]	RNDR	Indicates support for Random Number instructions in AArch64 state.  When FEAT_RNG_TRAP is implemented, the value returned by a direct read of ID_AA64ISAR0_EL1.RNDR is further controlled by the value of AArch64-SCR_EL3.TRNDR.  Defined values are: <b>0b0001</b> AArch64-RNDR and AArch64-RNDRS registers are implemented.	0b0001
[59:56]	TLB	Indicates support for Outer Shareable and TLB range maintenance instructions. Defined values are: <b>0b0010</b> Outer Shareable and TLB range maintenance instructions are implemented.	0b0010
[55:52]	TS	Indicates support for flag manipulation instructions. Defined values are: <b>0b0010</b> CFINV, RMIF, SETF16, SETF8, AXFLAG, and XAFLAG instructions are implemented.	0b0010
[51:48]	FHM	Indicates support for FMLAL and FMLSL instructions. Defined values are: <b>0b0001</b> FMLAL and FMLSL instructions are implemented.	0b0001
[47:44]	DP	Indicates support for Dot Product instructions in AArch64 state. Defined values are: <b>0b0001</b> UDOT and SDOT instructions implemented.	0b0001
[43:40]	SM4	Indicates support for SM4 instructions in AArch64 state. Defined values are: <b>0b0000</b> When the Cryptographic Extension is not implemented or is disabled or the SM3/SM4 Cryptographic instructions are disabled, then SM4 instructions are not implemented. <b>0b0001</b> When the Cryptographic Extension is implemented and the SM3/SM4 Cryptographic instructions are enabled, then SM4 instructions SM4E and SM4EKEY are implemented.	The reset values can be the following: 0b0000, 0b0001, respective to the value.

Bits	Name	Description	Reset
[39:36]	SM3	<p>Indicates support for SM3 instructions in AArch64 state. Defined values are:</p> <p><b>0b0000</b> When the Cryptographic Extension is not implemented or is disabled or the SM3/SM4 Cryptographic instructions are disabled, then SM3 instructions are not implemented.</p> <p><b>0b0001</b> When the Cryptographic Extension is implemented and the SM3/SM4 Cryptographic instructions are enabled, then SM3 instructions SM3SS1, SM3TT1A, SM3TT1B, SM3TT2A, SM3TT2B, SM3PARTW1, and SM3PARTW2 are implemented.</p>	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[35:32]	SHA3	<p>Indicates support for SHA3 instructions in AArch64 state. Defined values are:</p> <p><b>0b0000</b> When Cryptographic extensions are not implemented or disabled then SHA3 instructions are not implemented.</p> <p><b>0b0001</b> When Cryptographic extensions are implemented and enabled then SHA3 instructions EOR3, RAX1, XAR, and BCAX are implemented.</p>	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[31:28]	RDM	<p>Indicates support for SQRDMLAH and SQRDMLSH instructions in AArch64 state. Defined values are:</p> <p><b>0b0001</b> SQRDMLAH and SQRDMLSH instructions implemented.</p>	0b0001
[27:24]	TME	<p>Indicates support for TME instructions. Defined values are:</p> <p><b>0b0000</b> TME instructions are not implemented.</p> <p><b>When PSTATE.EL IN {EL2, EL1}</b> Access to this field is: <b>RAZ/WI</b></p> <p><b>When PSTATE.EL == EL1 and EL2Enabled()</b> Access to this field is: <b>RAZ/WI</b></p> <p><b>Otherwise</b> Access to this field is: <b>RO</b></p>	0b0000
[23:20]	Atomic	<p>Indicates support for Atomic instructions in AArch64 state. Defined values are:</p> <p><b>0b0010</b> LDADD, LDCLR, LDEOR, LDSET, LDSMAX, LDSMIN, LDUMAX, LDUMIN, CAS, CASP, and SWP instructions implemented.</p>	0b0010
[19:16]	CRC32	<p>Indicates support for CRC32 instructions in AArch64 state. Defined values are:</p> <p><b>0b0001</b> CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions are implemented.</p>	0b0001

Bits	Name	Description	Reset
[15:12]	SHA2	Indicates support for SHA2 instructions in AArch64 state. Defined values are:  <b>0b0000</b> When Cryptographic extensions are not implemented or disabled then SHA2 instructions are not implemented.  <b>0b0010</b> When Cryptographic extensions are implemented and enabled then SHA256H, SHA256H2, SHA256SU0, SHA256SU1, SHA512H, SHA512H2, SHA512SU0, and SHA512SU1 instructions are implemented.  When the CRYPTO configuration parameter is true and the CRYPTODISABLE input is low at reset Cryptographic Extensions are implemented	The reset values can be the following: 0b0000, 0b0010, respective to the value.
[11:8]	SHA1	Indicates support for SHA1 instructions in AArch64 state. Defined values are:  <b>0b0000</b> When Cryptographic extensions are not implemented or disabled then SHA1 instructions are not implemented.  <b>0b0001</b> When Cryptographic extensions are implemented and enabled then SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions are implemented.  When the CRYPTO configuration parameter is true and the CRYPTODISABLE input is low at reset Cryptographic Extensions are implemented	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[7:4]	AES	Indicates support for AES instructions in AArch64 state. Defined values are:  <b>0b0000</b> SVE2-AES instructions are not implemented. This value is reported when Cryptographic extensions are not implemented or are disabled.  <b>0b0010</b> SVE2 AESE, AESD, AESMC, and AESIMC instructions are implemented plus SVE2 PMULLB and PMULLT instructions with 64-bit source. This value is reported when Cryptographic extensions are implemented and enabled.  When the CRYPTO configuration parameter is true and the CRYPTODISABLE input is low at reset Cryptographic Extensions are implemented	The reset values can be the following: 0b0000, 0b0010, respective to the value.
[3:0]	RES0	Reserved	RES0

## Access

MRS <Xt>, ID\_AA64ISAR0\_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0110	0b000

## Accessibility

MRS <Xt>, ID\_AA64ISAR0\_EL1

```

if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
elseif PSTATE.EL == EL1 then

```



```
if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    X[t, 64] = ID_AA64ISAR0_EL1;
elseif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64ISAR0_EL1;
elseif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64ISAR0_EL1;
```

## 1.5 ID\_AA64ZFR0\_EL1, SVE Feature ID register 0

Provides additional information about the implemented features of the AArch64 Scalable Vector Extension instruction set, when one or more of FEAT\_SVE and FEAT\_SME is implemented.

For general information about the interpretation of the ID registers, see *Principles of the ID scheme for fields in ID registers* in the [Arm® Architecture Reference Manual for A-profile architecture](#).

### Configurations



Note

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

If FEAT\_SME is implemented and FEAT\_SVE is not implemented, then SVE instructions can only be executed when the PE is in Streaming SVE mode and the instructions are legal to execute in Streaming SVE mode.

### Attributes

#### Width

64

#### Functional group

Identification registers

#### Access type

See bit descriptions

#### Reset value

xxxx	0000	0000	xxxx	0001	xxxx	xxxx	xxxx	xxxx	0000	0001	0001	xxxx	xxxx	xxxx	0001
63	59	55	51	47	43	39	35	31	27	23	19	15	11	7	3 0

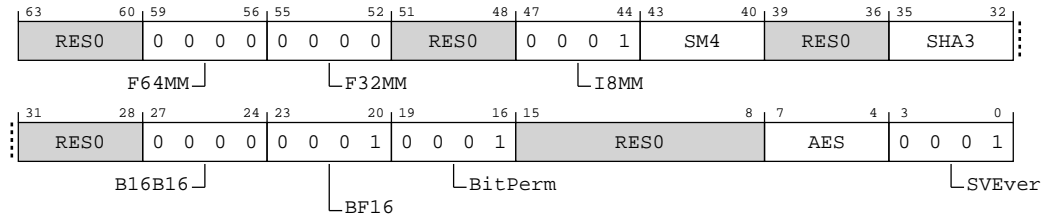


Note

Where the reset reads xxxx, see individual bits.

## Bit descriptions

**Figure 1-2: AArch64\_id\_aa64zfr0\_el1 bit assignments**



**Table 1-5: ID\_AA64ZFR0\_EL1 bit descriptions**

Bits	Name	Description	Reset
[63:60]	RES0	Reserved	RES0
[59:56]	F64MM	Indicates support for SVE FP64 double-precision floating-point matrix multiplication instructions. Defined values are:  <b>0b0000</b> Double-precision matrix multiplication and related SVE instructions are not implemented.	0b0000
[55:52]	F32MM	Indicates support for the SVE FP32 single-precision floating-point matrix multiplication instruction. Defined values are:  <b>0b0000</b> Single-precision matrix multiplication instruction is not implemented.	0b0000
[51:48]	RES0	Reserved	RES0
[47:44]	I8MM	Indicates support for SVE Int8 matrix multiplication instructions. Defined values are:  <b>0b0001</b> SVE SMMLA, SUDOT, UMMLA, USMMLA, and USDOT instructions are implemented.	0b0001
[43:40]	SM4	Indicates support for SVE SM4 instructions. Defined values are:  <b>0b0000</b> SVE2 SM4 instructions are not implemented. This value is reported when the Cryptographic Extension is not implemented or is disabled, or SM3/SM4 Cryptographic extensions are not implemented or are disabled.  <b>0b0001</b> SVE2 SM4E and SM4EKEY instructions are implemented. This value is reported when the Cryptographic Extension is implemented and SM3/SM4 Cryptographic instructions are enabled.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[39:36]	RES0	Reserved	RES0
[35:32]	SHA3	Indicates support for the SVE SHA3 instructions. Defined values are:  <b>0b0000</b> SVE2 SHA-3 instructions are not implemented. This value is reported when Cryptographic extensions are not implemented or are disabled.  <b>0b0001</b> SVE2 RAX1 instruction is implemented. This value is reported when Cryptographic extensions are implemented and enabled.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[31:28]	RES0	Reserved	RES0

Bits	Name	Description	Reset
[27:24]	B16B16	Indicates support for SVE2.1 non-widening BFloat16 instructions. Defined values are:  <b>0b0000</b> SVE2.1 non-widening BFloat16 instructions are not implemented.	0b0000
[23:20]	BF16	Indicates support for SVE BFloat16 instructions. Defined values are:  <b>0b0001</b> SVE BFCVT, BFCVTNT, BFDOT, BFMLALB, BFMLALT, and BFMMLA instructions are implemented.	0b0001
[19:16]	BitPerm	Indicates support for SVE bit permute instructions. Defined values are:  <b>0b0001</b> SVE BDEP, BEXT, and BGRP instructions are implemented.	0b0001
[15:8]	<b>RES0</b>	Reserved	<b>RES0</b>
[7:4]	AES	Indicates support for SVE AES instructions. Defined values are:  <b>0b0000</b> SVE2-AES instructions are not implemented. This value is reported when Cryptographic extensions are not implemented or are disabled.  <b>0b0010</b> SVE2 AESE, AESD, AESMC, and AESIMC instructions are implemented plus SVE2 PMULLB and PMULLT instructions with 64-bit source. This value is reported when Cryptographic extensions are implemented and enabled.	The reset values can be the following: 0b0000, 0b0010, respective to the value.
[3:0]	SVEver	Indicates support for SVE instructions when one or more of FEAT_SME and FEAT_SVE is implemented. Defined values are:  <b>0b0000</b> The SVE instructions are implemented.  <b>0b0001</b> As 0b0000, and adds the mandatory SVE2 instructions.  For this product, the selected value is 0b0001.	0b0001

## Access

MRS <Xt>, ID\_AA64ZFR0\_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0100	0b100

## Accessibility

MRS <Xt>, ID\_AA64ZFR0\_EL1

```

if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64ZFR0_EL1;

```

```
elseif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64ZFR0_EL1;
elseif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64ZFR0_EL1;
```

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PRE-1121-V1.0

# Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

## Product status

All products and Services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

### Product completeness status

The information in this document is Final, that is for a developed product.

### Product revision status

This product is r0p2, which indicates the revision status of the product described in this manual, where:

- r (value)** Identifies the major revision of the product, for example, r1.
- p (value)** Identifies the minor revision or modification status of the product, for example, p2.

## Revision history

These sections can help you understand how the document has changed over time.

### Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

#### Document history

Issue	Date	Confidentiality	Change
0002-06	27 September 2024	Non-Confidential	First release for r0p2
0001-05	13 March 2024	Non-Confidential	Second early access release for r0p1
0001-04	1 November 2023	Confidential	First early access release for r0p1
0000-03	27 March 2023	Confidential	First early access release for r0p0

The first table is for the first release. Then, each table compares the new issue of the manual with the last released issue of the manual. Issue numbers match the revision history in [Document release information](#) on page 15.

**Table 2: Issue 0000-03**

Change	Location
First early access release for r0p0	-
Editorial updates	Throughout document
Updated register information	<a href="#">1.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0</a> on page 5
Added register information	<a href="#">1.5 ID_AA64ZFR0_EL1, SVE Feature ID register 0</a> on page 9

**Table 3: Differences between Issue 0000-03 and Issue 0001-04**

Change	Location
First early access release for r0p1	-
Editorial updates	Throughout document
Updated register information	<a href="#">1.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0</a> on page 5
Added register information	<a href="#">1.5 ID_AA64ZFR0_EL1, SVE Feature ID register 0</a> on page 9

**Table 4: Differences between Issue 0001-04 and Issue 0001-05**

Change	Location
Second early access release for r0p1	-
Editorial updates	Throughout document
Product name change	Throughout document

**Table 5: Differences between Issue 0001-05 and Issue 0002-06**

Change	Location
First release for r0p2	-
Editorial updates	Throughout document
Moved content from frontmatter to backmatter	Throughout document
Updated product revision number	Throughout document
Updated register information	<a href="#">1.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0</a> on page 5
Updated register information	<a href="#">1.5 ID_AA64ZFR0_EL1, SVE Feature ID register 0</a> on page 9



# Conventions

The following subsections describe conventions used in Arm documents.

## Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: [developer.arm.com/glossary](https://developer.arm.com/glossary).

## Typographic conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
<i>italic</i>	Citations.
<b>bold</b>	Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments.  For example: <div>MRC p15, 0, &lt;Rd&gt;, &lt;CRn&gt;, &lt;CRm&gt;, &lt;Opcode_2&gt;</div>
SMALL CAPITALS	Terms that have specific technical meanings as defined in the <i>Arm® Glossary</i> . For example, <b>IMPLEMENTATION DEFINED</b> , <b>IMPLEMENTATION SPECIFIC</b> , <b>UNKNOWN</b> , and <b>UNPREDICTABLE</b> .



We recommend the following. If you do not follow these recommendations your system might not work.



Your system requires the following. If you do not follow these requirements your system will not work.



You are at risk of causing permanent damage to your system or your equipment, or of harming yourself.



This information is important and needs your attention.



This information might help you perform a task in an easier, better, or faster way.



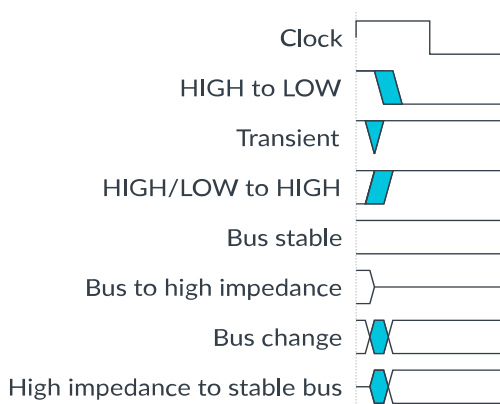
This information reminds you of something important relating to the current content.

## Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

**Figure 1: Key to timing diagram conventions**



## Signals

The signal conventions are:

### Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

## Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

# Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Access to Arm documents depends on their confidentiality:

- Non-Confidential documents are available at [developer.arm.com/documentation](https://developer.arm.com/documentation). Each document link in the following tables goes to the online version of the document.
- Confidential documents are available to licensees only through the product package.

Arm product resources	Document ID	Confidentiality
<i>Arm® Neoverse™ V3AE Core Configuration and Integration Manual</i>	101596	Confidential
<i>Arm® Neoverse™ V3AE Cryptography Extension (MP173) Release Note</i>	109899	Confidential
<i>Arm® Neoverse™ V3AE Core (MP172) Release Note</i>	109892	Confidential
<i><a href="#">Arm® Neoverse™ V3AE Core Technical Reference Manual</a></i>	101595	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
<i><a href="#">Arm® Architecture Reference Manual for A-profile architecture</a></i>	DDI 0487	Non-Confidential

Non-Arm resources	Document ID	Organization
<i>Advanced Encryption Standard (FIPS 197, November 2001)</i>	-	<a href="https://www.nist.gov">The National Institute of Standards and Technology (NIST)</a> <a href="https://www.nist.gov">www.nist.gov</a>
<i>Secure Hash Standard (SHS) (FIPS 180-4, August 2015)</i>	-	<a href="https://www.nist.gov">The National Institute of Standards and Technology (NIST)</a> <a href="https://www.nist.gov">www.nist.gov</a>
<i>Secure Hash Standard (SHS) (FIPS 202, August 2015)</i>	-	<a href="https://www.nist.gov">The National Institute of Standards and Technology (NIST)</a> <a href="https://www.nist.gov">www.nist.gov</a>